Claims 1, 15, 29 and 49-51 each recite a plurality of output circuits each of which outputs a respective data signal, a clock source and a plurality of adjustable delay circuits for receiving a first clock signal and for providing a respective delayed first clock signal to a respective one of said plurality of output circuits, "wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to the first clock signal [. . .] such that each of said respective data signals is output by said plurality of output circuits at substantially the same time."

Claim 41 recites receiving a plurality of data output signals, providing a first clock signal, generating respective applied clock signals and adjusting the delay of each of said respective applied clock signals such that the data output signals are output from . . . respective outputs of said output circuits at substantially the same time." Neither AAPA nor Ashuri, taken alone or in combination, teach or suggest the above-described limitations of claims 1, 15, 29, 41 and 49-51.

For example, while Ashuri appears to disclose clock shifting in an individual digital integrated circuit to account for different amounts of propagation delay (e.g., due to different amounts of logic circuits encountered) for a given data signal (See Ashuri at FIG. 3 and Abstract), Ashuri does not teach or suggest a plurality of adjustable delay circuits wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to a first clock signal such that a plurality if data signals are output by a respective plurality of output circuits at substantially the same time.

At best, Ashuri can been considered as disclosing nothing more than what is already disclosed in AAPA. For example, AAPA already discloses the use of a delay circuit 19 in between clock 17 and output buffer latch 13n. The reason why the delay circuit 19 is used in AAPA is to introduce a delay in the clock signal so that the data is delayed in being output from the latch 13n. This is precisely what Ashuri teaches, as acknowledged by the Office Action. For example, Ashuri discloses a delay shifter 310 in between an external clock 321 and an output of a flip flop 350. Ashuri at FIG. 3. That is, Ashuri

discloses nothing new to a person of ordinary skill in the art at the time of the invention. Therefore, combining AAPA with Ashuri does not lead a person of ordinary skill in the art at the time of the invention to the claimed inventions. At least for these reasons, claims 1, 15, 29, 41 and 49-51 are allowable over Ashuri and AAPA.

Claims 2, 5, 6, 10-13, 16, 19, 20, 24-27, 30, 33, 34, 38-40, 42, 43, 45-47 and 52 depend from claims 1, 15, 29 and 41 and are allowable at least for the reasons mentioned above in connection with claims 1, 15, 29 and 41 and also on their own merit.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

By

Thomas J. D'Amico
Registration No.: 28,371
Salvatore P. Tamburo
Registration No.: 45,153
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicant